Remarks

The Office Action dated March 15, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 5 and 7 have been amended, and claim 6 has been cancelled without prejudice. Accordingly, claims 1, 3-5 and 7 are pending in the present application and are respectfully submitted for consideration.

Claims 1 and 3-7 are Rejected Under 35 U.S.C. § 112

Claims 1 and 3-7 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claims 1, 5 and 7 have been amended responsive to the rejection, and thus are in compliance with US patent practice. Accordingly, Applicants respectfully request the rejection to be withdrawn.

Claims 1 and 3 Rejected Under 35 U.S.C. § 103(a)

Claims 1 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Heuner et al. (U.S. Patent No. 4,066,918, hereinafter "Heuner") in view of McDaniel (U.S. Patent No. 5,243,236). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor integrated circuit device comprising, among other features, a feedback circuit outputting to a gate of the first MOS transistor a value obtained by comparing a voltage at the second conductive region of the first MOS transistor with a reference voltage, wherein a load is connected to the second conductive region of the first MOS transistor, and wherein, between the first backgate

region and the second conducting region of the first MOS transistor, a first parasitic diode is formed and, between the second backgate region and the fourth conducting region of the second MOS transistor, a second parasitic diode is formed.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Heuner as allegedly disclosing "a first MOS transistor N1 having a first backgate region 305, a first conductive region 233, and a second conductive region 235, and having the first backgate region and the first conductive region thereof connected together; a second MOS transistor P1 having a second backgate region 330, a third conductive region 221, and a fourth conductive region 223 ..."

In addition, the Office Action stated that Heuner "do not teach first and second MOS transistors having the same polarity, and a load being connected to a connection portion between the first conductive region of the first MOS transistor and the third conductive region of the second MOS transistor," and characterized McDaniel as allegedly teaching "in figure 5 first and second MOS transistors having the same polarity."

Applicants submit that Heuner in view of McDaniel fail to disclose or suggest each and every element recited in claim 1 of the present application. In particular, it is submitted that the elements D_{P1}, D_{P2} and D_{N1}, D_{N2} of Heuner as well as MP1 and MP2 of McDaniel, are neither comparable nor analogous to that which is disclosed in the present invention.

For example, in the first MOS transistor of the present invention, the first backgate and the second conductive region together from the parasitic diode Dx2; and in the second MOS transistor of the present invention, the second backgate and the fourth conducting region together from the parasitic diode Dx1. The present invention provides the advantage of preventing a reverse current with these parasitic diodes Dx1 and Dx2 and to exploit the low on-state resistance of the first MOS transistor to reduce the voltage drop across it.

In contrast, the elements D_{P1} and D_{P2} of Heuner are formed between the source and drain, respectively, of the P-channel MOS transistor P1 and the substrate; and the elements D_{N1} and D_{N2} are formed between the source and drain, respectively, of the N-channel MOS transistor N1 and the N-type substrate 213. With these elements of Heuner, a reverse current cannot be prevented. Thus, Heuner's structure requires P- and N-channel MOS transistors.

Moreover, the backgate and source of the MOS transistor P1 in Heuner are connected via the diode D5 to the backgate and source of the MOS transistor N1.

In contrast, the sources of the two MOS transistors are connected together, but their drains are not in accordance to one example of the present invention. Moreover, Heuner states, in column 7, lines 5 to 34, that, when the diode D5 is reversely biased, the reverse bias voltage there remains constant and thereby protects the gates of the MOS transistors N1 and P1 from insulation breakdown. Heuner further states, in column 7, lines 60-61 that the diode D5 functions to limit the potential difference between the terminals 12 and 14.

The diode D5 of Heuner merely functions as a circuit for protection against insulation breakdown, and thus it is not solely by connecting together the backgate and source of the MOS transistor P1 and the backgate and source of the MOS transistor N1 that such protection is achieved. Applicants submit that this is different from the present invention because the present invention manages to prevent a reverse current with the parasitic diodes Dx1 and Dx2 and to exploit the low on-state resistance of the first MOS transistor to reduce the voltage drop across it.

Furthermore, McDaniel merely provides P-channel MOS transistors that are connected in series, namely the MOS transistor MP1, connected on the supply voltage Vpp side has the backgate and source thereof connected together, and namely the MOS transistor MP2, has the backgate and source thereof connected together.

This structure is for preventing breakdown (see Fig. 3 of McDaniel) that is caused by reverse connection between the n-well layer 362 and the p-type diffusion layer 361 serving as the drain of the MOS transistor MP2. Specifically, connecting the backgate of the MOS transistor MP2 to the node between the drain of the MOS transistor MP1 and the source of the MOS transistor MP2 helps prevent breakdown (see Fig. 5 of McDaniel) that is caused by reverse connection between the n-well layer 362 and the p-type diffusion layer 361 serving as the drain of the MOS transistor MP2.

In contrast, the present invention aims to prevent a reverse current with the parasitic diodes Dx1 and Dx2 and to exploit the low on-state resistance of the first MOS transistor to reduce the voltage drop across it. These aims cannot be achieved by the disclosure of McDaniel because the backgate of the MOS transistor MP1 is connected to the supply voltage Vpp in McDaniel. However, according to one example of the

present invention, the backgates of the first and second MOS transistors are connected to the region where the first and second MOS transistors are connected. Thus McDaniel's invention and the present invention are different also in how the backgate is connected.

In view of the above, Applicants submit that Heuner in view of McDaniel fail to disclose or suggest each and every element recited in claim 1 of the present application, and therefore is allowable.

As claim 3 depends from claim 1, Applicants submit that claim 3 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Heuner in view of McDaniel, alone or in combination, do not teach or suggest each feature recited by pending claims 1 and 3. Accordingly, for the above provided reasons, Applicants respectfully submit that pending claims 1 and 3 are not rendered obvious under 35 U.S.C. § 103 by the teachings of Heuner in view of McDaniel.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art

reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

Applicants respectfully request withdrawal of the rejection.

Claims 4 and 5 Rejected under 35 U.S.C. § 103(a)

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) in view of Heuner and McDaniel in view of Stewart (U.S. Patent No. 3,967). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Stewart is applied for allegedly teaching "a voltage setting circuit being composed of voltage division resistors." Stewart fails to cure the deficiencies noted above with respect to the rejection of claim 1. As claim 4 depends from claim 1, Applicants submit that claim 4 incorporates the patentable aspects therein, and is

therefore allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Claim 5 recites a semiconductor integrated circuit device comprising, among other features, an operational amplifier receiving at a non-inverting input terminal thereof a voltage at the second P-type diffusion layer of the first MOS transistor, receiving at an inverting input terminal thereof a reference voltage, and outputting to a gate of the first MOS transistor a value obtained by comparing the voltage at the second P-type diffusion layer with the reference voltage, wherein a load is connected to the second P-type diffusion layer of the first MOS transistor, and wherein, between the first backgate and the second P-type diffusion layer of the first MOS transistor, a first parasitic diode is formed and, between the second backgate and the fourth P-type diffusion layer of the second MOS transistor, a second parasitic diode is formed.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Heuner, McDaniel and Stewart are discussed above. It is submitted that Heuner in view of McDaniel and further in view of Stewart do not teach or suggest at least the above mentioned features above with respect to claim 5, and therefore Applicants submit that claim 5 is allowable.

Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1 and 3-5 and 7 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1 and 3-5 and 7 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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